WHAT IS CLAIMED IS:

1. A method of sequencing data transmission inside a computer system, wherein the computer system has a bridging device, a first bus and a second bus, and the bridging device further includes a second-to-first posted write buffer, the method comprising the steps of:

recording a plurality of write data stored inside the second-to-first posted write buffer when a first-to-second bus read operation via the bridging device occurs;

holding a response data obtained after executing the first-to-second bus read operation on the second bus; and

continuously transmitting the response data to the first bus after transmitting the write data to the first bus.

2. The method of claim 1, wherein the bridging device further provides a second-to-first flush flag buffer, contents thereof including state information of the write data stored inside the second-to-first posted write buffer.

3. The method of claim 2, wherein the system further provides a block logic for first-to-second read capable of sending out a control signal according to the state information.

4. The method of claim 3, wherein the bridging device further provides a hold buffer for first-to-second read for holding the response data and transmitting the response data to the first bus according to the control signal.

5. The method of claim 1, wherein the bridging device further provides a counter for storing a sum of the write data stored inside the second-to-first posted write buffer and decreasing by one when one write data transmitting to the first bus.

6. The method of claim 5, wherein the counter sends out a control signal as soon as the counter senses that all write data are already written.

7. The method of claim 6, wherein the bridging device further provides a hold buffer for first-to-second read for holding the response data and transmitting the response data to the first bus according to the control signal.

8. A bridging device coupled to a first bus and a second bus, comprising:

a posted write buffer for storing a plurality of write data transmitting from the second bus to the first bus; and

a hold buffer for holding a response data after executing a read operation on the second bus, and continuously transmitting the response data to the first bus after transmitting the write data, which are issued before the read operation, to the first bus.

9. The bridging device of claim 8, wherein the bridging device further includes a flush flag buffer, contents thereof including state information of the write data stored within the posted write buffer.

10. The bridging device of claim 9, wherein the bridging device further includes a block logic for read, capable of sending out a control signal according to the state information.

11. The bridging device of claim 10, wherein the hold buffer transmits the response data according to the control signal.

12. The bridging device of claim 8, wherein the bridging device further includes a counter for storing a sum of the write data, which are issued before the read operation, and decreasing by one when one write data transmitting to the first bus.

13. The method of claim 12, wherein the counter sends out a control signal as soon as the counter counts to zero.

14. A data transmission sequencing system, comprising:

a first bus;

a second bus; and

a bridging device, wherein after a read operation issued from the first bus to the second bus, the bridging device can hold a response data from the second bus, and the bridging device continuously transmits the response data to the first bus after a plurality of write data, which are issued before the read operation, transmitting to the first bus.

15. The system of claim 14, wherein the bridging device further comprises:

a posted write buffer for storing the write data; and

a hold buffer for holding the response data.

16. The system of claim 15, wherein the system further includes a flush flag buffer, contents thereof including state information of the write data stored within the posted write buffer.

17. The system of claim 16, wherein the system further includes a block logic for read capable of sending out a control signal according to the state information.

18. The system of claim 17, wherein hold buffer transmits the response data according to the control signal.

19. The system of claim 15, wherein the system further includes a counter for storing a sum of the write data, which are issued before the read operation, and decreasing by one when one write data transmitting to the first bus.

20. The system of claim 19, wherein the counter sends out a control signal as soon as the counter counts to zero.